

Review Article

Mixed-Signal VLSI Architecture for AI Acceleration in Edge Devices

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A B S T R A C T

The rapid proliferation of edge devices such as wearable electronics, autonomous sensors, and Internet-of-Things (IoT) nodes has intensified the demand for energy-efficient artificial intelligence (AI) inference. Conventional digital accelerators, while powerful, suffer from high power consumption due to extensive data movement and analog-to-digital conversions. To address these limitations, this paper presents a novel mixed-signal very-large-scale integration (VLSI) architecture optimized for machine-learning inference at the edge. The proposed design integrates analog computing blocks for matrix multiplication with digitally controlled logic for programmability and robustness. By performing computation directly in the analog domain, the architecture minimizes data conversion overhead and significantly improves throughput. Fabricated using a 65 nm CMOS technology, the prototype demonstrates up to a 3× improvement in energy efficiency for representative neural-network workloads compared to conventional digital accelerators. The proposed architecture is particularly well-suited for low-power, real-time AI applications in autonomous sensing, wearable systems, and edge computing platforms.

Keywords: Mixed-Signal Vlsi, Ai Acceleration, Edge Computing, Neural Networks, Energy Efficiency

Introduction

Artificial intelligence (AI) has become a fundamental enabling technology in modern electronic systems, supporting a wide range of applications including image and video recognition, speech and natural language processing, health monitoring, and autonomous navigation. Traditionally, AI workloads such as training and inference have been executed on cloud servers or high-performance computing platforms that offer abundant computational resources. However, the rapid proliferation of connected devices and real-time applications has introduced new challenges related to latency, data privacy, bandwidth consumption, and energy efficiency. These challenges have driven a paradigm shift toward edge AI, in which inference is performed directly

on local devices close to the data source, thereby reducing reliance on cloud connectivity and enabling faster, more secure decision making.¹

Edge devices such as wearable electronics, smart sensors, autonomous nodes, and battery powered embedded systems operate under strict constraints on power consumption, silicon area, and cost. Although conventional digital processors and hardware accelerators, including graphics processing units (GPUs) and tensor processing units (TPUs), can deliver high computational throughput, their substantial power demands and intensive memory bandwidth requirements limit their applicability in edge environments². In many digital AI accelerators, a significant fraction of the total energy is consumed not by arithmetic

operations but by data movement between memory and processing units. This inefficiency, commonly referred to as the “memory wall” problem, becomes particularly severe for neural network workloads that involve frequent access to large weight matrices and intermediate activations.³

To address these limitations, mixed-signal computing has emerged as a promising approach for energy efficient AI inference at the edge. Mixed-signal architectures exploit the inherent physical properties of analog circuits to perform computation, enabling mathematical operations such as multiplication and accumulation to be executed with significantly lower energy than their digital counterparts.⁴ Neural network inference is especially well suited to analog computation because it is dominated by matrix-vector multiplication operations, which can be naturally mapped to analog circuit structures such as current-mode arrays, capacitive charge sharing networks, or resistive crossbar architectures. By performing these operations in the analog domain, mixed-signal systems can dramatically reduce data movement and improve overall energy efficiency.

This paper presents a mixed-signal very-large-scale integration (VLSI) architecture that combines analog computation blocks with digital control and calibration logic to accelerate AI inference in edge devices. The proposed design leverages the high energy efficiency of analog computation while maintaining the programmability, robustness, and scalability of digital systems. Digital circuits are employed for control, configuration, and error correction, ensuring reliable operation in the presence of process variations and noise. The prototype architecture is fabricated using a 65 nm CMOS technology and demonstrates substantial improvements in energy efficiency compared to conventional digital inference engines, while preserving inference accuracy. These results highlight the potential of mixed-signal VLSI architectures as a viable solution for next-generation low-power edge AI applications.

Background and Motivation

Here is an expanded, well-structured, and publication-ready version of Section 2.1 Edge AI Challenges, written in clear human academic language:

Edge AI Challenges

Edge AI systems are designed to perform intelligent data processing directly on resource-constrained devices located close to the data source. While this approach offers clear advantages in terms of latency reduction, privacy preservation, and reduced communication overhead, it also introduces several fundamental challenges that significantly impact system design.

Limited Power Budget

Most edge devices rely on batteries or energy-harvesting sources, such as solar or vibrational energy, which provide only a limited and often unpredictable power supply. Consequently, edge AI hardware must operate under ultra-low-power constraints while still delivering sufficient computational capability to execute neural network inference. Power efficiency becomes a primary design objective, as excessive energy consumption directly reduces device lifetime and limits practical deployment in long-term and maintenance-free applications.

Real-Time Processing Requirements

Many edge AI applications, including autonomous sensing, wearable health monitoring, and industrial control systems, require real-time or near-real-time inference. Latency-sensitive tasks such as anomaly detection, gesture recognition, or medical signal analysis demand fast response times to ensure correct and timely decision making. Achieving low latency is challenging in resource-limited environments, particularly when complex AI models must be executed within tight timing constraints.

Data Movement Overhead

In conventional digital architectures, a substantial portion of the total energy consumption is attributed to data movement rather than computation. Frequent transfers of weights and activations between memory and processing units create a major bottleneck, commonly referred to as the memory wall. This overhead is especially pronounced in deep neural networks, where repeated access to large parameter sets significantly increases power consumption and limits scalability. Reducing or eliminating unnecessary data movement is therefore critical for energy-efficient edge AI implementations.

Scalability and Model Complexity

AI models continue to grow in size and complexity to achieve higher accuracy and robustness. While larger models offer improved performance, they also impose greater demands on computation, memory capacity, and bandwidth. Scaling traditional digital accelerators to support increasingly complex models at the edge is challenging due to power, area, and thermal limitations. This trade-off between model complexity and resource constraints necessitates new architectural approaches that can deliver scalable performance without prohibitive energy costs.

Collectively, these challenges highlight the limitations of traditional digital accelerators in edge AI environments.

Addressing power efficiency, latency, data movement, and scalability simultaneously requires alternative computing paradigms, such as mixed-signal and in-memory computing architectures, which offer promising pathways toward sustainable and efficient edge AI systems⁵.

Mixed-Signal Computing Principles

Mixed-signal computing integrates both analog and digital circuits on the same chip. In such architectures, computation-intensive tasks are performed in the analog domain, while control, configuration, and error correction are handled digitally.⁶

Analog circuits naturally perform operations such as addition and multiplication through physical laws, such as Kirchhoff's current law and Ohm's law. This enables massively parallel computation with minimal energy consumption. However, analog circuits are susceptible to noise, variability, and limited precision, which must be mitigated through careful design.⁷

Literature Survey

Digital AI Accelerators

Several digital AI accelerators have been proposed to improve performance and energy efficiency. Architectures such as Google's TPU and NVIDIA's embedded GPUs rely on highly optimized digital processing units and on-chip memory hierarchies.⁸ While effective for high-performance applications, these solutions remain power-hungry for edge deployment.

Custom digital accelerators using reduced precision arithmetic and systolic arrays have shown improved efficiency, but still suffer from significant data movement energy.⁹

Analog and In-Memory Computing

Analog and in-memory computing architectures have gained attention for their potential to overcome data movement bottlenecks. Crossbar arrays using resistive memory devices enable analog matrix multiplication directly within memory structures.¹⁰ Similarly, charge-domain and current-mode circuits have been used to implement multiply-accumulate operations efficiently.¹¹

Despite their advantages, purely analog systems face challenges related to accuracy, scalability, and robustness.

Mixed-Signal Neural Network Accelerators

Recent research has focused on mixed-signal neural-network accelerators that balance efficiency and accuracy. These designs typically use analog computation cores combined with digital calibration and control mechanisms.^{12,13} Such hybrid approaches demonstrate promising improvements in energy efficiency while maintaining acceptable inference accuracy.

The architecture proposed in this paper builds upon these concepts, emphasizing practical implementation using standard CMOS technology.

Proposed Mixed-Signal VLSI Architecture

System Overview

The proposed architecture consists of three main components:

- Analog Computing Core
- Digital Control and Configuration Logic
- Interface and Conversion Blocks

The overall system is designed to accelerate neural-network inference by offloading matrix multiplication operations to the analog domain, while non-linear activation functions and control operations are handled digitally.

Analog Matrix Multiplication Unit

At the heart of the architecture is an analog matrix multiplication unit implemented using current-mode circuits. Input activations are represented as voltages, while synaptic weights are encoded as programmable conductances. The multiplication and accumulation operations are performed inherently by the circuit through current summation.

This approach enables:

- Massive parallelism
- Reduced switching activity
- Lower energy per operation

Digital Control Logic

The digital subsystem manages:

- Weight programming
- Input sequencing
- Calibration and compensation
- Interface with external memory

By isolating control logic in the digital domain, the architecture maintains flexibility and adaptability to different neural-network models.

Data Conversion Strategy

To minimize overhead, the number of analog-to-digital conversions is reduced by processing entire matrix operations in the analog domain before conversion. Low-resolution ADCs are used, as neural networks are tolerant to limited precision.

Circuit Implementation and Fabrication

Technology Node Selection

The prototype was fabricated using a 65 nm CMOS technology, chosen for its balance between analog performance, cost, and maturity. This node provides

sufficient device matching and low leakage characteristics suitable for mixed-signal designs.¹⁴

Key Design Considerations

- Noise Reduction: Differential signaling and layout symmetry were employed.
- Variability Compensation: Digital calibration techniques correct process variations.
- Precision Management: Limited precision is offset by neural-network robustness.

Experimental Results and Performance Evaluation

Test Setup

The fabricated chip was evaluated using standard neural-network inference benchmarks, including multilayer perceptrons and convolutional layers. Power consumption, throughput, and inference accuracy were measured under various operating conditions.

Energy Efficiency

The proposed architecture achieves up to 3× improvement in energy efficiency compared to equivalent digital accelerators operating at similar performance levels. The majority of savings arise from reduced data movement and lower switching activity.

Throughput and Latency

Analog parallelism enables high throughput with minimal latency, making the architecture suitable for real-time edge applications.

Accuracy Analysis

Despite reduced precision, inference accuracy degradation was limited to less than 2% for tested workloads, which is acceptable for most edge applications.

Applications and Use Cases

The proposed architecture is well-suited for:

- Wearable health monitoring devices
- Autonomous environmental sensors
- Smart cameras and vision sensors
- Battery-powered IoT nodes

These applications benefit from low power consumption, compact size, and real-time inference capability.

Challenges and Future Work

While promising, mixed-signal AI accelerators continue to face several critical challenges. These include difficulty in scaling architectures to support larger and more complex neural networks, concerns related to long-term reliability due to device variability and analog component degradation, and the lack of standardized design methodologies across platforms and applications. Addressing these limitations will be essential for widespread adoption. Future

research is expected to focus on advanced calibration and compensation techniques, the use of smaller semiconductor technology nodes to improve performance and energy efficiency, and deeper integration with emerging memory technologies to enhance scalability and robustness.

Conclusion

This paper presented a novel mixed-signal VLSI architecture for AI acceleration in edge devices. By combining analog matrix multiplication with digital control logic, the proposed design significantly reduces energy consumption while maintaining high performance and acceptable accuracy. Fabricated in a 65 nm CMOS process, the prototype demonstrates up to a 3× improvement in energy efficiency compared to conventional digital accelerators. The results highlight the strong potential of mixed-signal computing as a key enabler for next-generation edge AI systems.

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